MATRIX
Maven Academy for Technology, Research, Innovation & eXcellence

WOOLF

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Student Academic Record

Master of Science in VLSI Design and Embedded Systems

Full name: **Tomáš Garrigue Masaryk**
Nationality: **Poland**
Student ID: **0000000000**
Degree name: **Master of Science in VLSI Design and Embedded Systems**
Degree accreditation level: **ECTS Accredited (EQF7)**
Degree completion status: **Completed**
Date of award: **03 June 2026**
Official accreditation information: **Degree listing on MFHEA website in Europe**
Average (percent): **100%**
Cumulative GPA: **4**

Course title	Completed	Hours	ECTS credits	US percent	GPA
Tier 2:					
Introduction to Machine Learning	03/06/2026	125	5	100%	4
Advanced Embedded System Design - Part 1	03/06/2026	125	5	100%	4
Intelligent systems	03/06/2026	125	5	100%	4
Advanced VLSI Design - Part 2	03/06/2026	125	5	100%	4
Robotics and automation	03/06/2026	125	5	100%	4
Advanced VLSI Design - Part 3	03/06/2026	125	5	100%	4
Advanced IC Manufacturing, Packaging and Testing - Part 1	03/06/2026	125	5	100%	4
Advanced SoC	03/06/2026	125	5	100%	4
Advanced Embedded System Design - Part 2	03/06/2026	125	5	100%	4
Linux and Shell Scripting	03/06/2026	125	5	100%	4
Advanced Computer Architecture	03/06/2026	125	5	100%	4
Computer Architecture - Part 2	03/06/2026	125	5	100%	4
Advanced VLSI Design for Testing - Part 2	03/06/2026	125	5	100%	4

Course title	Completed	Hours	ECTS credits	US percent	GPA
Design Automation	03/06/2026	125	5	100%	4
Advanced VLSI Design - Part 1	03/06/2026	125	5	100%	4
Advanced IC Manufacturing, Packaging and Testing - Part 2	03/06/2026	125	5	100%	4
Advanced VLSI Physical Design and Verification - Part 2	03/06/2026	125	5	100%	4
Advanced Embedded System Design - Part 3	03/06/2026	125	5	100%	4
Hands-on-Labs	03/06/2026	125	5	100%	4
Advanced VLSI Design Verification - Part 2	03/06/2026	125	5	100%	4
Advanced VLSI Physical Design and Verification - Part 1	03/06/2026	125	5	100%	4
Advanced VLSI Design for Testing - Part 1	03/06/2026	125	5	100%	4
SoC Design - Part 2	03/06/2026	125	5	100%	4
Prompt Engineering	03/06/2026	125	5	100%	4
Pilot Project	03/06/2026	125	5	100%	4
Emerging Artificial Intelligence Technologies	03/06/2026	125	5	100%	4
Advanced VLSI Design Verification - Part 1	03/06/2026	125	5	100%	4
Physical Design	03/06/2026	125	5	100%	4
Design For Testing	03/06/2026	125	5	100%	4
Design Verification	03/06/2026	125	5	100%	4
Tier 3:					
Introduction to Machine Learning	03/06/2026	125	5	100%	4
Advanced Embedded System Design - Part 1	03/06/2026	125	5	100%	4
Intelligent systems	03/06/2026	125	5	100%	4
Capstone Project	03/06/2026	250	10	100%	4
Advanced VLSI Design - Part 2	03/06/2026	125	5	100%	4
VLSI Design - Part 2	03/06/2026	125	5	100%	4
Robotics and automation	03/06/2026	125	5	100%	4

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Course title	Completed	Hours	ECTS credits	US percent	GPA
Advanced VLSI Design - Part 3	03/06/2026	125	5	100%	4
Computer Architecture - Part 1	03/06/2026	125	5	100%	4
Advanced IC Manufacturing, Packaging and Testing - Part 1	03/06/2026	125	5	100%	4
Advanced SoC	03/06/2026	125	5	100%	4
Advanced Embedded System Design - Part 2	03/06/2026	125	5	100%	4
Linux and Shell Scripting	03/06/2026	125	5	100%	4
Advanced Computer Architecture	03/06/2026	125	5	100%	4
Computer Architecture - Part 2	03/06/2026	125	5	100%	4
Embedded System Design - Part 1	03/06/2026	125	5	100%	4
Advanced VLSI Design for Testing - Part 2	03/06/2026	125	5	100%	4
Design Automation	03/06/2026	125	5	100%	4
Advanced VLSI Design - Part 1	03/06/2026	125	5	100%	4
VLSI Design - Part 1	03/06/2026	125	5	100%	4
SoC Design - Part 1	03/06/2026	125	5	100%	4
Advanced IC Manufacturing, Packaging and Testing - Part 2	03/06/2026	125	5	100%	4
Advanced VLSI Physical Design and Verification - Part 2	03/06/2026	125	5	100%	4
Advanced Embedded System Design - Part 3	03/06/2026	125	5	100%	4
Hands-on-Labs	03/06/2026	125	5	100%	4
Advanced VLSI Design Verification - Part 2	03/06/2026	125	5	100%	4
Advanced VLSI Physical Design and Verification - Part 1	03/06/2026	125	5	100%	4
Embedded System Design - Part 2	03/06/2026	125	5	100%	4
Advanced VLSI Design for Testing - Part 1	03/06/2026	125	5	100%	4
SoC Design - Part 2	03/06/2026	125	5	100%	4
Prompt Engineering	03/06/2026	125	5	100%	4
Pilot Project	03/06/2026	125	5	100%	4

Course title	Completed	Hours	ECTS credits	US percent	GPA
Emerging Artificial Intelligence Technologies	03/06/2026	125	5	100%	4
Advanced VLSI Design Verification - Part 1	03/06/2026	125	5	100%	4
Physical Design	03/06/2026	125	5	100%	4
Design For Testing	03/06/2026	125	5	100%	4
Design Verification	03/06/2026	125	5	100%	4
Tier 1:					
VLSI Design - Part 2	03/06/2026	125	5	100%	4
Computer Architecture - Part 1	03/06/2026	125	5	100%	4
Embedded System Design - Part 1	03/06/2026	125	5	100%	4
VLSI Design - Part 1	03/06/2026	125	5	100%	4
SoC Design - Part 1	03/06/2026	125	5	100%	4
Embedded System Design - Part 2	03/06/2026	125	5	100%	4
Introduction to Artificial Intelligence	03/06/2026	125	5	100%	4
		2250	90	100%	4

Transcript issued and signed on 03 June 2026 by:

Dr. Joshua Broggi
President

Sivakumar P R
Dean of MATRIX - Maven Academy for Technology, Research, Innovation & eXcellence

Student credentials

europass

This Diploma Supplement follows the model developed by the European Commission, Council of Europe and UNESCO/CEPES. The purpose of the supplement is to provide sufficient independent data to improve the international 'transparency' and fair academic and professional recognition of qualifications (diplomas, degrees, certificates etc.). It is designed to provide a description of the nature, level, context, content and status of the studies that were pursued and successfully completed by the individual named on the original qualification to which this supplement is appended. It should be free from any value judgements, equivalence statements or suggestions about recognition.
Information in all eight sections should be provided. Where information is not provided, an explanation should give the reason why.

1. Information identifying the holder of the qualification

1.1. Full name: Tomáš Garrigue Masaryk

1.2. Date of birth (dd/mm/yyyy): 03/06/2026

1.3. Student identification number: 0000000000

2. Information identifying the qualification

2.1. Name of qualification and (if applicable) title conferred (in original language):
Master of Science in VLSI Design and Embedded Systems

2.2. Main field(s) of study for the qualification: Computer & Mathematical Science

2.3. Name and status of awarding institution (in original language): Woolf

2.4. Name and status of institution (in different from 2.3) administering studies:
Woolf (established in 2018) is an accredited Higher Education Institution in Malta with license 2019-015 from the Malta Further and Higher Authority.

2.5. Language of instruction/examination: English

3. Information on the level and duration of the qualification

3.1. Level of qualification: ECTS Accredited (EQF7)

3.2. Standard Programme Length: 18 months

3.3. Standard Programme Delivery Length: 18 months

3.4. Access requirements: Undergraduate Degree or Equivalent

4. Information on the programme completed and the results obtained

4.1. Programme learning outcomes:

Knowledge
a) Describe and explain fundamental concepts in VLSI design, embedded systems, and digital hardware architectures, including CMOS principles, RTL design, and
microcontroller/microprocessor fundamentals as demonstrated through analytical assignments, and design documentation.
b) Critically evaluate design methodologies, EDA tools, and automation techniques for front-end and back-end chip development, by producing documented analyses of power, performance, and area (PPA) trade-offs using industry-standard tools.
c) Explain and justify strategies for integrating embedded systems with VLSI components, including hardware-software co-design and system-on-chip (SoC)
architectures supported by case studies or system-block diagrams

d) Assess and report on emerging trends in semiconductor technologies, design automation, and embedded system applications, with a focus on scalability, low-power design, and real-world mplementation using structured reports grounded in current literature and industry benchmarks.
e)Identify and apply relevant professional, security, sustainability, and hardware-design standards (e.g., IEEE 1800, IEEE 1687, ISO 26262, RISC-V specs) in the contextof VLSI and embedded system applications, as evidenced in assignments and project documentation.
f) Analyse emerging hardware architectures and accelerator-based systems, including virtualised platforms, GPUs, and NPUs, in the context of modern
VLSI and embedded system design.

Skills

A. Core Skills (Applicable to All Graduates)

a) Design and implement digital hardware and embedded system components using industry-standard HDLs and-programming languages, and simulate, debug and verify designs using professional toolchains.
b) Develop and evaluate integrated hardware-software systems through modelling, testing, and validation in real and simulated environments.
c) Optimise digital and system-level designs for performance, power efficiency, scalability, and reliability using synthesis, verification, timing analysis and place-and-route techniques.
d) Apply scripting, automation, and version control tools (e.g., Python, TCL, Shell, Git) to manage, document and-streamline complex design workflows and verification processes.
e) Apply applied research methods in VLSI and embedded systems contexts, including problem formulation, literature and standards review, experimental design, data collection, analysis of simulation or prototype results, and technical reporting.
f) Plan, manage, and execute complex VLSI or embedded systems projects autonomously, making informed technical decisions, managing time and resources, mitigating design risks, and delivering validated solutions aligned with professional and industry standards.

B. Pathway-Specific Advanced Skills

In addition to the core skills, graduates develop advanced competencies aligned with their chosen elective pathway.

1. VLSI Design & Verification Path

Graduates following this pathway will additionally be able to:
g) Design complex RTL architectures and implement advanced digital subsystems for ASIC/FPGA targets.
h) Develop and execute structured verification strategies using simulation, testbench development, and assertion-based methodologies.
i) Analyse and resolve timing, power, and signal integrity issues in advanced digital designs.
j) Apply formal verification and validation techniques to ensure functional correctness and design robustness.

2. Embedded & SoC Systems Path

Graduates following this pathway will additionally be able to:
g) Architect and integrate heterogeneous system-on-chip (SoC) platforms combining processors, accelerators, and peripherals.
h) Develop low-level firmware and optimise hardware-software co-design for real-time and embedded applications.
i) Evaluate system-level trade-offs involving latency, memory hierarchy, power constraints, and communication protocols.
j) Implement secure and scalable embedded architectures for industrial or application-specific deployment.

3. Manufacturing, Testing & Physical Design Path

Graduates following this pathway will additionally be able to:
g) Apply physical design methodologies including placement, routing, floorplanning, and layout optimisation.
h) Perform design-for-test (DFT) implementation and fault coverage analysis.
i) Analyse manufacturability constraints, yield optimisation, and reliability considerations in silicon production.
j) Evaluate advanced node design challenges, including power integrity, clock distribution, and thermal considerations.
The differentiation between core and pathway-specific skills ensures that all graduates meet MQF Level 7 expectations for autonomy, complexity, and applied research competence, while also developing advanced specialist expertise aligned with their chosen technical domain.

Competencies

a) Demonstrate the ability to collaborate effectively in multidisciplinary teams, integrating knowledge of hardware,-software, and system-level design.
b) Exhibit creativity and innovation in solving design challenges, contributing to advancements in chip design, embedded systems, and automation frameworks.
c) Apply ethical reasoning and professional standards in VLSI and embedded system projects, ensuring designs are secure, reliable, and socially responsible.
d) Demonstrate continuous professional development through the independent acquisition and critical evaluation of emerging tools, technologies, standards, and methodologies in semiconductor and embedded systems design, integrating new knowledge into project work and professional practice.
e) Lead and manage projects in VLSI and embedded systems, overseeing the design cycle, resource management, and delivery of reliable and efficient solutions.

4.2. Programme details, individual credits gained and grades/marks obtained: Refer to the first page of this transcript

4.3. Grading system and, if available, grade distribution table: Refer to the first page of this transcript.

5. Information on the function of the qualification

5.1. Access to further study: Degree Programmes may entitle access to EQF8 Level Study

5.2. Access to a regulated profession (if applicable): Not Applicable

6. Additional information

6.1. Further information sources: **https://woolf.education/regulation/regulatory-resources**

7. Certification of the supplement

7.1. Transcript issued and signed on 03 June 2026 by:

7.2.

Dr. Joshua Broggi
President

7.3.

Sivakumar P R
Dean of MATRIX - Maven Academy for Technology, Research, Innovation & eXcellence

7.4. Official stamp or seal:

GPA	US grade	US percent	UK mark	UK classification	Malta grade	Malta mark	Malta classification	Swiss grade
4	A+	97-100	70+	First class honours	A	80-100%	First class honours	6
3.9	A	94-96	67-69	Upper-second class honours	B	70–79%	Upper-second class honours	
3.7	A-	90–93	65–67	Upper-second class honours				5.5
3.3	B+	87–89	60–64	Lower-second class honours	C	55–69%	Lower-second class honours	
3	B	84–86						
2.7	B-	80–83	55–59	Lower-second class honours				5
2.3	C+	77–79	50–54	Third class honours	D	50–54%	Third class honours	
2	C	74–76						
1.7	C-	70–73	45–49	Third class honours				4.5
1.3	D+	67–69	40–44	Ordinary/unclassified				
1	D	64–66	35–39	Ordinary/unclassified				
0.7	D-	60–63						4
0	F	Below 60	Below 35		F	45–54%		1-3.5